DfX Glossary of Terms

This Glossary of Terms is courtesy of Alfred Crouch from his book:
Design for Test for Digital IC's and Embedded Core Systems

A-B C-D E-F G-H I-J K-L M-N O-P Q-R S-T U-V W-Z

A-B

AC Fault Models:
mathematical descriptions of faulty behavior designed to assess timing compliance of a circuit -- the most common examples are the gate-level transition and the path delay fault models.

AC Testing:
the application of vectors to a circuit with the intent to verify the timing compliance -- for example, testing using the transition or path delay fault models to determine the delay or cycle-time involved in conducting register-to-register, input-to-register, and register-to-output transfers.

ATPG (Automatic Test Pattern Generation):
the use of a software tool to generate test vectors algorithmically.

At-Speed Scan:
a scan test architecture that allows the scan chains to be operated (shift and sample) at the rated clock frequency for purposes of verifying timing criteria (frequency, specifications, AC faults), and to reduce the tester application time.

Automatic Test Equipment (ATE):
a class of equipment used to apply vectors to a completed chip design -- also known as a tester, test platform, IC ATE. A tester may be used to test final packaged product, or it may be used in conjunction with other support equipment such as wafer probers to conduct test on raw die.

Benchmarking:
the comparison of items against a “best in class” standard, or against each other with a “selection criteria” established. This term, in the context of this text, is applied in two ways: it is applied to the process of comparing various ATPG tools, with an established selection criteria, to choose the tool that best meets the needs of the design or test organization; and it is applied to the process of comparing embedded cores, with an established selection criteria, to choose the core that best meets the needs of the design organization.

BIST (Built-in Self-Test):
a design unit generally with on-chip resources to apply stimulus and evaluate responses so that the design unit can be tested to some level from within the chip (for example, memory BIST allows a memory test unit to be placed on-chip, for the purpose of testing the on-chip embedded memory arrays, with minimum direct interaction from an external tester). BIST is commonly described in two main categories, Logic BIST and Memory BIST.

BIST'ed Memory:
a memory array with a BIST methodology closely associated -- more specifically, one with the BIST logic in close association so the physical unit may be treated as a single design entity, with associated signals such as Data, Address, Read-Write, Output-Enable, BIST-Invoke, BIST-Done, and BIST-Fail (as opposed to, for example, a single centralized BIST controller that has the ability to test multiple memory arrays).

BIST Test Wrapper:
a design unit or level of hierarchy, that is viewed as the external interface of a non-mergeable or “test-in-isolation” core, that uses embedded built-in self-test techniques, such as LFSR's for pattern generation (PRPG) and/or response evaluation (Signature Analysis), as the method to apply and/or evaluate isolated testing.

Bridging Fault Model:
a fault model represented by shorting together two elements -- these elements can be transistor components and connections, gate components and connections, or

wire interconnect signals. The case of an element being constantly shorted to power (VDD) or ground (VSS) is the stuck-at fault model.

C - D

Circuit Learning:
a process conducted by the ATPG tool to identify complex circuits, or structures that are difficult to operate or make tracing decisions through, and to establish the way to deal with these circuits prior to beginning algorithmic test generation. Circuit learning reduces the time involved with vector generation, or enhances the ability of the ATPG engine to successfully create a vector.

Clock Domain:
all sequential elements connected to the same physical clock distribution network -- note that a chip design may have multiple domains and some domains may be defined to be operated at the same frequency, however, if the physical clock nets are distributed separately with different skew and delay management, then they are considered different clock domains.

Combinational:
a type of circuit or circuit description that is comprised only of combinational gates -- there is no state holding logic, sequential logic, or memory logic in the circuit description. In the context of this text, circuits rendered effectively combinational simplify the ATPG process.

Concurrent Test Engineering:
the methodology whereby the test issues, concerns, goals, and budgets of a chip design are dealt with concurrently to the functional design. The opposing methodology has been called “over the wall” in that the design is accomplished and then it is “tossed over the wall” to a test group to then eke out the quality measurement on the completed and frozen design.

Controllability:
the ability to place nets, nodes, gates, or sequential elements to a known logic state. This has two main contexts in this text, the ability for an ATPG tool to place known

values wherever necessary in the design description during the vector generation activity; and the ability for a tester to place known values at the edge of a chip, or within a chip by using a test architecture such as scan.

Core: see Embedded Core

Cost-of-Test:

the measurement of the expense generated during a chip design, or of the cost added to a final chip product, due to the DFT or test process. In the context of this text, the cost-of-test is described as the additional time added to the design cycle due to DFT and test activities (TTM impact); the additional time added to the product cycle due to vector generation for qualification time -- time-to-volume (TTV impact); the direct impact to the silicon size due to test logic (Silicon Cost); the direct impact to the number of package pins and to power rating of a chip package due to test logic (Packaging Cost); and the direct costs involved with the testing process such as the cost of the tester, the throughput time on a test floor, the cost and complexity of the test program, etc. (Test Cost). These costs can be separated into recurring and non-recurring costs, where recurring costs are incurred each time a final chip is produced.

Critical Path:

those paths that establish the product's frequency, or pin specifications, within some defined timing guardband, and those paths that would establish the product's frequency in the presence of delay faults that would not be caught by some other test such as stuck-at or transition delay based testing.

Current-Based Fault Model:

a fault model that may be represented by any of the structural, bridging, or delay fault models, that is applied with the intent of measuring the current drawn by the circuit as the observe operation, rather than the propagation of voltage values to observe points.

DC Fault Models:

mathematical descriptions of faulty behavior designed to assess structural compliance of a circuit independent of any timing requirements -- the most common example is the gate-level stuck-at fault model.

Defects:
the “real world” physical anomalies that can occur in silicon or in packaging. Defects may result in the final chip product not being in compliance with it's operation parameters (logic functions, frequency performance, power consumption), or may result in a limited product lifetime (reliability). Defects may exist, but may not be destructive -- not all defects map to fault models and ultimately chip failure modes.

Delay-Based Fault Model:
mathematical representations of faulty behavior based on the concept of timing. In the context of this text, the launching of a voltage-based logic transition (0->1, 1->0) into a circuit, and the observance of the circuits logic response to that transition at a later time interval. The most common examples of delay-based fault models are the gate-level transition and path delay models.

Delay Fault Models: see Path Delay and Transition Delay entries.

Delay Path Sensitization:
the establishing of a propagation pathway from one point in a circuit to another point in a circuit, through a described pathway of gate elements, by controlling the “off path” values of the gate elements in the path -- for example, the AND type gate would have a logic 1 placed on the off-path gate inputs to allow the path-input to pass the logic 1 or logic 0 value. This analysis is done by an ATPG tool during the generation of path delay vectors.

Design Rules for Test: also known as DFT rules
the set of design restrictions placed on a design description for the test process. These rules are applied to ease the vector generation process (manual or ATPG); to enhance the quality measurement metric (fault coverage); or to reduce the cost-of-test (test time, vector depth). Common design rule examples are: no asynchronous sequential elements, no combinational feedback paths; no non-scannable sequential elements.

Deterministic Vector Generation:

a type of ATPG where all vectors that are created are crafted deterministically by targeting faults and algorithmically generating a unique vector to exercise the fault and propagate the fault effect to an observe point. The other form of vector generation is “random”, where random groupings of logic 1's and 0's are applied and fault coverage is assessed by fault simulation.

DFATPG: Design-for-ATPG
the action of applying design rules to a chip design to ensure that an ATPG tool can successfully generate vectors and achieve a targeted quality level.

DFT: Design-for-Test
the action of placing features in a chip design during the design process to enhance the ability to generate vectors, achieve a measured quality level, or reduce the cost-of-test.

E - F

Edge Set: see Tester Edge Sets.

Embedded Core: a reusable design unit, meant to be integrated as part of a larger design, that can be delivered as a soft core (HDL and RTL), firm core (gate-level netlist), or hard core (layout description). The core can be further grouped as mergeable (the core can be mixed and merged or flattened with other logic), and non-mergeable (the core is meant to be delivered and integrated as a complete unit and “tested-in-isolation”).

Exhaustive Testing:
a test method whereby all possible 2n values are applied to the inputs of a combinational circuit to exercise every possible applied value. For sequential circuits, this method requires the application of all possible 2n values to the inputs, and the application of all possible 2m sequential sequences of the 2n values.

Expected Response:
the predicted or deterministic output of a circuit under test. When a circuit in a known state is exercised by a known input stimulus, the cared outputs (real

response) must match the expected response -- any difference between the real response and the expected response is a failure.

Failure:
a real vector response that is measured at the tester and compared to the predicted “expected response”. Any differences between the real response and the expected response is a failure and is the criteria used to discard silicon product. Although vectors are applied to exercise faults, a successfully exercised fault that is propagated to a tester observe point is called a failure.

Fault Coverage:
the metric of how many faults are exercised and successfully detected (their fault effect is observed) versus the total amount of fault content in the circuit under test.

Fault Dropping:
the part of the ATPG process where the tool removes detected faults from the total list of faults contained in the circuit. This is a tool runtime and a vector sizing optimization operation.

Fault Equivalence:
the part of the ATPG process where the ATPG tool conducts fault management by declaring the equivalent faults to a fundamental fault and then removes equivalent faults from the fault list. Equivalent faults are those that are automatically detected when a fundamental fault is exercised -- for example, detecting the stuck-at 0 fault on the output of an AND-gate requires driving the output to a logic 1, which requires driving all inputs to a logic 1, thereby detecting the stuck-at 0 faults on all inputs.

Fault Exercising:
the portion of a vector that excites the fault. In the context of this text, an ATPG tool will place a fault in a design description, and will trace back from the fault location to the necessary control points to create the portion of the vector that will excite the fault (drive it to the opposite of it's faulted value for a stuck-at fault, or apply a logic transition for a delay fault).

Fault Grading: also known as vector grading

the act of simulating a target vector against a good circuit description, and a circuit description that contains a fault -- the goal being to see if the expected response is different between the two circuits at an observe point. If a difference is detected, then the fault has been detected -- if a difference is not detected, then the fault is masked for that vector (not detected).

Fault Masking:
a fault that is not able to be detected due to a circuit configuration problem such as reconvergent fanout or redundancy. An exercised fault can not be driven uniquely to an observe point.

Fault Metric:
the measurement of the fault content of a circuit -- see fault coverage.

Fault Model:
a mathematical model of faulty behavior that can be used to assess the compliance of a circuit to various criteria. For example, structural compliance can be verified by using a stuck-at fault model, timing compliance can be verified by using a delay fault model, and current leakage compliance can be verified by using a bridging fault model.

Fault Selection:
the part of the ATPG process where the tool selects a fault from the total list of faults contained in the circuit.

Fault Simulation: see fault grading.
Full-Scan: a scan test architecture in which all sequential elements, that are not specialized memory cells, are scan cells connected into scan chains -- and proper logic precautions have been taken to allow for the ability to safely shift random logic values through the scan chains.

Functional Testing:
a form of testing where a design element is tested by the application of functional, operational, or behavioral vectors. In general these vectors are graded for structural

coverage when applied to the final product testing. If the vectors are not structurally graded, then the testing may be called “design verification”.

G - H

I - J

Iddq Testing: quiescent current testing
a form of testing where an IC is placed in a state and after the combinational switching has settled, the current drawn by the IC is measured. In CMOS processes, good transistors draw no current other than diode reverse current when the transistor is not actively switching.

JTAG Test Wrapper:
a test wrapper that uses, and maintains compliance with, the boundary scan architecture, TAP, and TAP controller described in the IEEE 1149.1 Standard. A JTAG test wrapper uses a “slow scan” method that allows functional vectors to be serialized, scanned into the interface, and then applied “all at once” with an update operation. JTAG test wrappers generally do not support the needs of at-speed test or AC test goals. JTAG is mostly associated with the chip package pin interface, and not individual cores.

Input Stimulus:
the applied logic values to a circuit under test.

K - L

Logic BIST:
a form of testing for logic circuits where the stimulus generator and/or the response verifier is placed within the circuit. The most common form of logic BIST is to use linear feedback shift registers (LFSR's) to conduct pseudo-random pattern generation (PRPG) and to conduct output pattern compression (signature analysis).

Known State:

a requirement in order to conduct testing. A circuit under test must have a known state so that a deterministic (predictable) response can be generated by the application of a known input stimulus.

M - N

Manufacturing Testing:
testing accomplished after the manufacture of a silicon product. The purpose of this testing is to verify that the manufacturing process did not add destructive defect content to the chip design. This type of testing is generally applied to packaged parts to ensure that the packaging process also did not add destructive defect content to the final product.

Mostly Full-Scan:
a partial-scan test architecture where most of the sequential elements, other than specialized memory cells, are scan cells and are connected into scan chains. The sequential cells that are not made scannable are those that are in areas of critical timing where scan insertion would negatively impact chip performance, or large register arrays where scan insertion would negatively impact the chip area budget.

Multiplexor Mode:
a method of connecting an embedded core, with or without a test wrapper, to the package pins of the part for access to test operations -- this term is generally applied to an embedded core that does not support any other form of testing but the application of functional design vectors through the functional interface, or through a bus interface, brought out to the package pins.

Non-Recurring Cost:
the “one time” cost incurred on a silicon product. In the context of this text, it is the cost-of-test that is added to the product during the design-for-test development and the vector generation process.

O - P

Observability:

the ability to observe nets, nodes, gates, or sequential elements after they have been driven to a known logic state. This has two main contexts in this text, the ability for an ATPG tool to drive fault effects to observe points in the design description during the vector generation; and the ability for a tester to observe expected response values of the chip internals at the package pins.

Parallel Scan:
the architectural support of multiple scan chains, that are designed to be used simultaneously, to reduce the number of shift clocks (shift bit depth) involved with the scan process by parallelizing the scan bit depth across several tester channels. This architecture reduces the required clock cycles needed to load a state in the design unit and reduces one aspect of the cost-of-test.

Parametric Testing:
a form of testing where the

Partial-Scan:
a scan test architecture which allows sequential elements other than specialized memory cells, to not be scan cells, and to not be connected into existing scan chains. Only some cells are made scannable and connected into scan chains -- usually only those cells that restrict the ability to achieve a high fault coverage metric.

Path Delay Fault Model:
a mathematical model of faulty behavior that relies on a complete logic pathway being slow-to-rise or slow-to-fall as the fault, and is used to verify the timing compliance of a circuit pathway. This is accomplished by driving the fault to the fail value initially, and then by applying a logic transition, and by observing the propagated fault effect at a later time interval.

Path Sensitization:
the establishing of a propagation pathway from one point in a circuit to another point in a circuit to propagate a fault effect to an observe point. This analysis is done by an ATPG tool during the generation of vectors.

Pattern:

a grouping of individual vectors. Usually the grouping of vectors has a purpose such as “the logic verification pattern”, “the memory test pattern”, or the “input leakage pattern”. Sometimes vectors are grouped into small pattern sets to fit within the memory limits of a test platform, and several of these patterns collectively make up a purposeful pattern such as “the logic verification pattern set”.

Pin Specifications:
the timing specifications involved with the ability to apply new data to chip input pins, and to observe valid chip output data. The specifications are usually defined as input-setup, input-hold, output-valid, and output-hold.

Q - R

Quality:
a term associated with the overall goodness of a part. In the test industry, this term is taken as meaning the measurable fault coverage of a delivered device plus the device's reliability statistics.

Reliability:
a term associated with the defect-free lifetime of a product (how long does the product last in the field before it fails due to a latent defect). The metric for reliability is generally a mean-time-between-failures (MTBF) rating or a failures-in-time (FIT) rating.

Symantec System Works
-- Installed – generally will automatically defend against virus attack
the cost that is incurred and repeated each time a product is manufactured. In the context of this text, it is the cost-of-test incurred with each device -- the DFT logic impact to each die and the “in socket” test time for each product that is tested.

Retention Testing:
a form of testing to assess whether the state elements (sequential and memory) of a circuit are able to retain logic state for a long period of time. This form of testing is done routinely on memory arrays, and is sometimes accomplished on sequential logic elements if the design is advertised as “static”.

Robust Fault Detection:
a term applied to delay testing where a path is exercised uniquely, and all off-path values required to enable the propagation path being tested, are held stable for the number of time intervals required to conduct the test. For example, a two-cycle test that launches a 0->1 transition into a path must have all off-path logic values remain stable for the two cycles -- if the off-path values toggle, then the resulting transition at the observe point may not be uniquely due to the launched transition.

S - T

Scan Cell:
a sequential element connected as part of a scan chain -- in the context of this text, a D flip-flop, having a scan multiplexor to allow selection between the functional D input and the test-only SDI input. Scan flip-flops, when in functional mode, may support all specialty sequential functions such as Set, Reset/Clear, Data Hold, Clock Enable, and Asynchronous functions, however, it is recommended that the scan function has the higher priority than all other flip-flop functions.

Scan Chain:
a set of scan cells connected into a shift register by connecting the scan cell ‘s Q, or SDO, output port to the dedicated SDI scan input port.

SDI:
the Scan Data Input port on a scan cell -- more specifically, the assert side of the input multiplexor when the control signal, SE, is asserted.

SDO:
the dedicated Scan Data Output port on a scan cell, or the connection on the scan cell Q or QB output port used as a dedicated scan connection to another scan cell's SDI port.

Scan Domain:
a set of scannable flip-flops that are connected and synchronized by the same clock, and are controlled by the same scan enable -- for designs with multiple clock

domains, there are multiple scan domains that can be shifted and sampled independent of each other, and can be operated in such a way as to preserve the natural timing relationship between clock domains if necessary.

Scan Mode:
the configuration of a design unit that supports the use of the scan chains for test purposes -- more specifically, a test encoding allows applied scan data to be read into the first scan element of certain scan chains, allows test data to be read from the last element of certain scan chains, and allows the scan enable signal to be used to control the shift or sample action of certain scan chains -- other internal control signals may also be created and asserted. A signal named “scan mode” is sometimes created to constrain certain pins and circuit elements during scan testing.

Scan Test Wrapper:
a design unit or level of hierarchy, that is viewed as the external interface of a non-mergeable or “test-in-isolation” core, that uses scan chains routed through the interface hierarchy level, and/or test access to internal scan chains, as the method to apply and evaluate isolated embedded testing.

SE:
the scan enable port on a scan cell and it's globally routed control signal -- this is the multiplexor control signal that selects whether the scan cell will update with data from the functional D input port or the test-only SDI input port -- this signal is generally distributed as a fanout tree since it must control every scannable flip-flop in a design.

SE -- Fast_SE, Slow_SE, Shift_SE:
when multiple clock domains exist, multiple scan enable signals, SE, must exist to provide independent shift and sample control of portions of the design and to create the independent scan domains -- for example, Fast_SE would be the scan enable (SE) signal distributed to all scannable flip-flops connected to the fast clock., while PLL_SE would be the scan enable signal distributed to the scan chains in the Phased-Lock-Loop design element.

SE -- Force_SE, Tristate_SE:

when scan design rules are relaxed on asynchronous elements, gated-clocking, and tristate or multiple driver nets, then scan control signals are needed to ensure safe shifting can occur (scan data is not stopped or corrupted during the shift operation, and driven contention does not occur during the shift operation). These signals may not fanout to every scan flip-flop, and so, they should be modeled in the HDL/RTL and synthesized to make timing as opposed to SE signals which are gate-level scan inserted.

Sequential:
a type of circuit or circuit description that is comprised of both combinational gates and state holding or sequential logic in the circuit description. In the context of this text, circuits that are sequential require multiple time frame combinational ATPG, or sequential ATPG, to process.

Serendipitous:
In the context of this text, this is bonus fault coverage that is discovered when a vector for a targeted fault is fault simulated. For example, a vector is created to target only one fault, when this vector is fault simulated it is discovered that 30 other faults were detected -- the 30 extra faults are serendipitous fault coverage. Another form of serendipitous fault coverage is when vectors generated against one fault model are graded against another fault model -- for example, a set of vectors with 97% stuck-at fault coverage are fault simulated against the transition delay fault model and 35% serendipitous fault coverage is discovered.

Shared Pins, Borrowed Pins:
package pins that have extra uses other than their functional purposes -- more specifically, in the context of this text, pins that are used to provide direct access to scan chains or direct access to embedded core units when those units are in a test mode.

Single Fault Assumption:
the assumption that an ATPG engine or a fault simulator uses to simplify their processes. It is much easier to conduct the various analyses with only one fault installed in the design description -- including the ability to conduct analyses with multiple faults significantly increases the compute resources needed.

Structural Testing:
a form of testing whereby the goal is to verify the structure of a chip (the wire connections and the gate truth tables). The opposing form of testing is functional or behavioral testing.

Stuck-At Fault Model:
a mathematical representation of faulty behavior that is modeled by shorting gate connections and wire routes to either VDD or VSS. The SAF is a DC fault model that is applied independent of timing or frequency.

Test:
the observation of a known expected response as a result of the application of a known input vector into a circuit in a known state -- the purpose being to measure some effect against a compliance standard.

Testability: see Design-for-Testability

Test Coverage:
a metric that is slightly different than fault coverage. Test coverage can be defined as the cumulative fault coverage of the testable logic (non-testable or redundant faults are removed from the denominator). Test coverage is generally higher than fault coverage.

Tester Accuracy:
the smallest ambiguity there is in edge placement.

Tester Edge Sets:
a tester timing format that can be applied to each pin individually. An edge set, for example, is the data format and timing information involved with applying new data to a chip input pin, and is comprised of the input-setup time, the input-hold time, and the waveform type such as NR or RTZ. A chip package pin may support more than one edge set.

Tester Precision:

the smallest measurement that the tester can resolve.

Tester Timing Format:
a term related to tester vector formats. Testers may contain waveform generators that make use of various waveform types such as non-return (NR), return-to-zero (RZ), surround-by-complement (SBC) which are designed to change logic values at the setup and hold times associated with an input pin. A test pattern comprised of logic 1's and 0's can be mapped to these various formats during the development of the test program. These timing formats are designed to verify the device pin specifications with each vector application.

Test Program:
a collection of test patterns that have been organized in a certain order and converted to the language of a specific test platform. It is called a program because it is basically software, and the tester is the CPU -- test patterns may be comprised of subroutines, pattern and test routine calls, and algorithmically controlled or sequenced events.

Test Wrapper:
a design unit or level of hierarchy, that is viewed as the external interface of a non-mergeable or “test-in-isolation” core, that also contains logic that allows isolated testing to occur -- the testing supported can be BIST, Scan, or direct access from multiplexed pins. A test wrapper is usually designed to reduce the functional interface of a core to a more manageable number of test signals, to ease test integration.

Time-to-Market: TTM
the amount of time it takes to get from a design specification to a product sample. Time-to-market generally concerns the design aspect of a product development cycle.

Time-to-Volume: TTV
the amount of time it takes to get a chip into volume production. Time-to-volume generally concerns the vector delivery, tester management, and yield enhancement aspects of the development cycle.

Transition Delay Fault Model:
a mathematical model of faulty behavior that is based on a gate or gate connection being slow-to-rise or slow-to-fall, and is used to verify the timing compliance of that gate or gate connection. This is accomplished by driving the fault to the fail value initially, and then by applying a logic transition, and by observing the propagated fault effect at a later time interval.

U - V

Vector:
the collection of logical 1's and 0's applied to a chip at a given point in time. Usually the vector is referenced from a synchronizing clock signal -- in this case, the definition of a vector is the collection of logical 1's and 0's applied per clock edge. Scan vectors are a special case in where a single scan vector is the collection of logical 1's, 0's, and clocks required to load a scan chain.

Vector Efficiency:
also known as “fault efficiency” or “fault efficient vectors” -- a metric that concerns the “faults per clock-cycle”, or the fault coverage content of a vector set in relation to the size of the vector set. A rating of more faults-per-vector is generally good, but a higher rating indicates vectors with high activity content which may consume more power during application.

Vector Masking:
the ability to ignore an “expected response value” of an output vector. In the context of this text, this has two applications, the ability of an ATPG tool to print vectors in a data format that includes a vector mask (a pseudo-vector that maps onto an output vector and indicates which bits of the vector are “cared”); the ability of the test platform to ignore output values that are not required as part of the test on a vector-by-vector basis.